



Docket No.: J&R-0694

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By: Th P.

Date: 11/26/01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Thomas Zettler  
Applic. No. : 09/922,479  
Filed : August 3, 2001  
Title : Method and Device for Testing an Integrated Circuit, Integrated Circuit to be Tested, and Wafer with a Large Number of Integrated Circuits to be Tested  
Art Unit : 2133

RECEIVED  
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Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents and Trademarks,  
Washington, D.C. 20231

Sir:

In accordance with 37 C.F.R. 1.98 copies of the following patents and/or publications are submitted herewith:

United States Patent No. 5,241,266 (Ahmad et al.), dated August 31, 1993;

United States Patent No. 5,388,104 (Shirotori et al.), dated February 7, 1995;

United States Patent No. 5,570,374 (Yau et al.), dated October 29, 1996;

European Patent Application EP 0 492 624 A1 (Shirotori et al.), dated July 1, 1992;

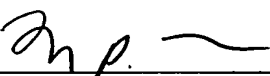
European Patent Application EP 0 568 239 A2 (Yau), dated November 3, 1993;

Japanese Patent Abstract JP 00 124 279 A (Nakada et al.), dated April 28, 2000;

Rangarajan, Sampath et al.: "Built-In Testing of Integrated Circuit Wafers", IEEE Transactions on Computers, Vol. 39, No. 2, February 1990, pp. 195-205.

If no translation of pertinent portions of any foreign language patents or publications mentioned above is included with the aforementioned copies of those applications, patents and/or publications, it is because no existing translation is readily available to the applicant.

Respectfully submitted,

  
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For Applicant

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